**Online Workshop on “FPGA Prototyping of VLSI Designs using High-Level Synthesis”**

**Topic:** FPGA Prototyping of VLSI Designs using High-Level Synthesis

**Date:** 10 / 10 / 2020

**Time:** 2:30 PM to 4:00 PM

**Speaker:**

**Mr. Prateek Sikka**

SoC Emulation Manager,

NXP Semiconductors, Noida, U.P., India

**About the Workshop:**

FPGAs are gaining importance in VLSI design flow for faster execution of verification tests and as platforms of choice for software development in pre-silicon. HLS tools are also getting popular among VLSI designers and architects due to design cycle time reduction they offer because of higher level abstraction and behavioural IP re-use. In this session, we will discuss how one can use HLS flows to implement and optimize designs and target them for FPGAs like Xilinx.  During the session, we will also discuss how to leverage continuous verification of the designs which is a typical feature offered by HLS tools.

**Brief Profile of the speaker:**

**Research Areas:**

Digital systems design and optimizations, FPGA prototyping and emulation, and high level synthesis

**Professional Experience:**

March, 2017 – Current: NXP Semiconductors, Noida (Emulation and FPGA prototyping for SoC designs)

Oct, 2016 – March, 2017: Cadence Design Systems (Low Power and Power Aware Emulation Engineer)

July, 2015 – Oct, 2016: MathWorks India Pvt. Ltd (Sr. Application Engineer, HDL Code Generation and Signal processing)

Jun, 2012 – July, 2015: Mentor Graphics India Pvt Ltd (Lead Application Engineer, Emulation and solutions)

Jun, 2006 – Jun, 2012: STMicroelectronics India (Emulation Engineer for SoCs)

**Education:**

B.E. (Electronics and Communication, Thapar University, Patiala) (2002- 2006)

M.Tech. (Integrated Electronics, IIT Delhi) (2007- 2010) (In collaboration with STMicroelectronics)

**Other Activities and achievements:**

* Multiple journal and conference publications in the area of work
* Guest Faculty, Shiv Nadar University, Greater Noida (2015- Current)
* Guest faculty, IIIT Delhi Masters research project co-supervision (2015- 2016).
* Multiple workshops and faculty development programmes conducted at Institutes in India: DRDO Delhi, Hyderabad, Space Applications Center, Ahmedabad, Delhi Technological University, Defense Institute of Advanced Technologies, Pune, MNNIT Allahabad.